Amendments to the Specification

Please amend the specification as follows:

In the paragraph starting at the bottom of Page 14, please make the following changes:

For example, FIG. 3C is a block diagram of an alternative embodiment for the transmit and receive path circuitry of a digital phased array module having time delay control of ADC and DAC sampling rates according to the present invention. In this embodiment, a single control register 350 and common time delay circuitry 356 are utilized for both the ADC 108 and the DAC 112. The delay value 352, therefore, controls the clock signal 358 (SCLK+DELAY) that is sent to both the ADC 108 and the DAC 112. This clock signal 358 (SCLK+DELAY) includes the clock signal (SCLK) 360 provided by clock circuitry 110 plus a programmable time delay added by time delay circuitry 356. The clock signal ~~358 (SCLK+DELAY)~~ 360 (SCLK) is also provided to registers 214 and 314 that are utilized to synchronize the transmit and receive signals. In this architecture, therefore, the same time delay is applied to the receive path ADC and the transmit path DAC such that the receive and transmit beams would have the same shape and main lobe orientation.